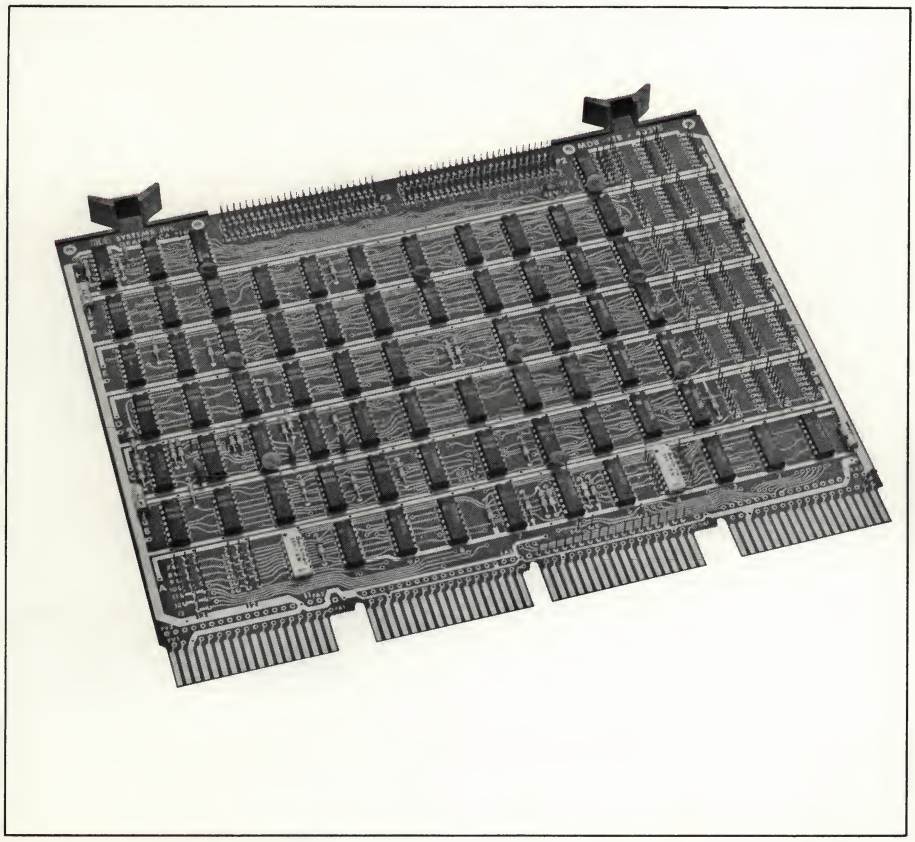
MDB 11B GENERAL PURPOSE DMA CONTROLLER

for use with PDP*-11 Computers



- low-cost PDP-11* Unibus* to-peripheral DMA control
- including essential controller logic plus facilities to add user's peripheral interface
- add up to 12 IC devices
- fits one slot of BB-11 or DD11 peripheral mounting panel

The MDB-11B General Purpose Direct Memory Access Controller Module interfaces a DEC PDP-11 Unibus* with a user's peripheral. The module consists of mounted IC devices plus wire-wrap facilities for up to 12 user-added IC devices, on a single quad board. The module accommodates 14-pin or 16-pin devices in wire-wrap sockets, or directly mounted.

The MDB-11B includes logic to perform six essential tasks in DMA transfer: that is, address selection, interrupt control, bus master control, word counting, and input and output data buffering.

The user utilizes the available wire-wrap facilities on the module to mechanize a command and status register for his specific application.

User input and output signals are TTL-compatible and available at two ribbon cable connectors. The connectors may be used as I/O cables to external devices, or for interconnection between the MDB-11B and other compatible MDB modules.

Address Selection Logic

Addresses are decoded to select the internal word count register, bus address register, data input and output registers, or the user-designed command and status register, for output to the Unibus interface. Logic includes receivers, inverters, decoder, and logic to provide a synchronizing pulse under control of an external master device.

The registers are decoded in four sequential addresses from 760000 through 777770. Ten input lines may be strapped through wire-wrap posts to form the enabling address to the decoder.

A sequence of output sync pulses is provided to notify the PDP-11 of device addressing, and for loading registers, etc., after the user address is detected and the master device asserts the pulse MSYNL.

Interrupt Control Logic

Interrupt control logic provides a vectored interrupt request to the PDP-11 processor. Wire-wrap jumper conections determine the address (4 through 374), and the bus request level (4 through 7).

The interrupt request initiates the bus request sequence on the selected bus request line. The resulting input bus grant signal informs the user's inter-

face that the interrupt sequence has begun and the interrupt request may be removed.

If the user's interface is not busy, the interrupt sequence issues control signals and causes the vector-select signal to gate the jumper-selected address into data lines 2 through 7.

Bus Master Control

This logic permits the user's interface to make the MDB-11B act as the bus master in order to perform a DMA transfer operation. A user-generated signal produces a bus request, which elicits a bus grant signal. The bus grant signal permits this logic to notify the user interface that the bus cycle is in progress.

Bus Address Register

The 15-bit bus address register specifies the bus address for direct bus access. It supplies 15 bits to the address bus, while the user's interface supplies three additional bits. Two control signals permit incrementing the register once for byte addressing, or twice for sequential word addressing, for each cycle.

Word Count Register

This 16-bit register is loaded with the complement of the number of words to be transferred, and then incremented to zero by the user's interface. The zero count is detected and the resulting signal is accessible at a wire-wrap post.

Input Data and Output Data Registers

The 16-bit output data register makes data available at the user's interface for transfer to the user's device. The input data register, controlled by the user's interface, makes data from the user's device available at the Unibus.

Data Line Multiplexer and Unibus Interface

The data line multiplexer transfers the bus address, word count, data, or the contents of the user-designed command and status register, to the Unibus. The multiplexer is controlled by the two least-significant bits of the device address, which are decoded to select the appropriate information for transfer. Information is strobed to the Unibus drivers when the device address is detected.

Outputs of Unibus receivers are accessible at wire-wrap posts for connection to the user's interface logic.

Electrical Requirements

- +5V at 1.7A

Accessories

- Optional general purpose cables available

Physical

- Occupies one quad slot of standard system unit

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